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☐ 1. Document ID: US 6535307 B1

Using default format because multiple data bases are involved.

L5: Entry 1 of 6 File: USPT Mar 18, 2003

US-PAT-NO: 6535307
DOCUMENT-IDENTIFIER: US 6535307 B1

TITLE: Method and apparatus for display of imaging parameters

DATE-ISSUED: March 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Allen; Roy D.	Burlington	MA		
Romano; David J.	Lowell	MA		
Hinds; Stephen C.	Andover	MA		

US-CL-CURRENT: 358/504; 358/406

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Ima

☐ 2. Document ID: US 5781308 A

L5: Entry 2 of 6 File: USPT Jul 14, 1998

DOCUMENT-IDENTIFIER: US 5781308 A
TITLE: High speed system for threshold matrix alignment and tiling, during creation of a binary half-tone image

Application Filing Date (1):
19960304

Detailed Description Text (46):
Note that when the threshold matrix is tiled to coincide with the destination image resolution, there may be an offset in the ending bytes (if each threshold row is not an integer sub-multiple of the destination image). In such a case, the threshold matrix byte values at the end of a row in SRAM are "filled in" to assure a concurrent ending of both the threshold matrix row and the destination image. For example, during clock cycle 4, bytes A and B are used to fill in the word which is entered into pipeline register 222.

Current US Original Classification (1):
358/451

Current US Cross Reference Classification (1):
358/3.23

Current US Cross Reference Classification (2):
358/528

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Ima

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☐ 3. Document ID: US 5778158 A

L5: Entry 3 of 6 File: USPT Jul 7, 1998

DOCUMENT-IDENTIFIER: US 5778158 A
TITLE: High speed system for image scaling

Application Filing Date (1):
19960304

Detailed Description Text (45):
Note that when the threshold matrix is tiled to coincide with the destination image resolution, there may be an offset in the ending bytes (if each threshold row is not an integer sub-multiple of the destination image). In such a case, the threshold matrix byte values at the end of a row in SRAM are "filled in" to assure a concurrent ending of both the threshold matrix row and the destination image. For example, during clock cycle 4, bytes A and B are used to fill in the word which is entered into pipeline register 222.

Current US Original Classification (1):
358/1.2

Current US Cross Reference Classification (1):
358/1.1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Ima

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☐ 4. Document ID: US 5771105 A

L5: Entry 4 of 6 File: USPT Jun 23, 1998

DOCUMENT-IDENTIFIER: US 5771105 A
TITLE: High speed system for grey level image scaling, threshold matrix alignment and tiling, and creation of a binary half-tone image

Application Filing Date (1):
19960304

Detailed Description Text (44):
Note that when the threshold matrix is tiled to coincide with the destination image resolution, there may be an offset in the ending bytes (if each threshold row is not an integer sub-multiple of the destination image). In such a case, the threshold matrix byte values at the end of a row in SRAM are "filled in" to assure a concurrent ending of both the threshold matrix row and the destination image. For example, during clock cycle 4, bytes A and B are used to fill in the word which is entered into pipeline register 222.

Current US Original Classification (1):
358/2.99

☐ 5. Document ID: US 5594839 A

L5: Entry 5 of 6 File: USPT Jan 14, 1997

DOCUMENT-IDENTIFIER: US 5594839 A
TITLE: Apparatus and method for improving black and color separation in halftoned images by printing black dots in a different screen phase

Application Filing Date (1):
19941017

Detailed Description Text (31):
The line offset of the ROM the address is applied to ROM lookup table 738, via line 736, by modulo circuit 730. Modulo circuit 730 also generates a repeating output which repeats with a frequency equal to the number of rows in the dither array. Modulo circuit 730 is driven, in turn, by a start-of-line signal (SOL) from address generator 714, provided via lead 726. Address generator 714 applies the SOL signal to line 726 at the start of each scan line. Thus, the line offset applied to ROM lookup table 738 will increase with each scan line of input pixel values until the number of rows in the dither array has been processed at which point, the threshold values in the dither array will be reused. This reusing effectively causes the dither array threshold values to be "tiled" over the image values.

Current US Original Classification (1):
358/1.9

Current US Cross Reference Classification (2):
358/536

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Ima

☐ 6. Document ID: US 5267054 A

L5: Entry 6 of 6 File: USPT Nov 30, 1993

DOCUMENT-IDENTIFIER: US 5267054 A
** See image for Certificate of Correction **
TITLE: Method and apparatus for the reduction of memory space required for a digital halftone system

Application Filing Date (1):
19910626

Current US Original Classification (1):
358/3.2

Current US Cross Reference Classification (1):
358/465

CLAIMS:

11. The method according to claim 1, wherein the step of retrieving a threshold value from the threshold array further comprises retrieving a threshold value from the threshold array for rendering a pixel at (x,y) coordinates (dx,dy), comprising the steps of:

determining the location of dy relative to the number of rows of threshold arrays, n, from the threshold array at the (0,0) location;

setting an offset to be equal to the number of threshold values in a row of tiles, the number of the row of tiles being equal to the height of the threshold array, said offset indicating the number of threshold values the threshold array is shifted for each subsequent row of threshold arrays;

generating an (x,y) index (dx',dy') into the threshold array to retrieve the threshold value for generating said display signal which renders the pixel at coordinated (dx,dy) utilizing the following equations:

dx'=(dx-n*offset) mod (w)

dy'=(dy-n*h)

where h is the height of the threshold array, w is the width of the threshold array and mod is a modular function.

20. The apparatus according to claim 14, wherein said accessing means for retrieving a threshold value from the threshold array for rendering a pixel at (x,y) coordinates (dx,dy), comprising:

means for determining the location of dy relative to the number of rows of threshold arrays, n, from the threshold array at the (0,0) location;

means for setting an offset to be equal to the number of threshold values in a row of tiles, the number of the row of tiles being equal to the height of the threshold array, said offset indicating the number of threshold values the threshold array is shifted for each subsequent row of threshold arrays;

means for generating an (x,y) index (dx', dy') into the threshold array to retrieve the threshold value to render the pixel at coordinated (dx, dy) utilizing the following equations:

dx'=(dx-n*offset) mod (w)

dy'=(dy-n*h)

where h is the height of the threshold array, w is the width of the threshold array and mod is a modular function.

21. The apparatus according to claim 14, further comprising accessing means for retrieving a threshold value from the threshold array for rendering a pixel at (x,y) coordinates (dx, dy), comprising:

means for determining the location of dy relative to the number of rows of threshold arrays, n, from the threshold array at the (0,0) location;

means for setting an offset to be equal to the number of threshold values in a row of tiles, the number of the row of tiles being equal to the height of the threshold array, said offset indicating the number of threshold values the threshold array is shifted for each subsequent row of threshold arrays;

means for generating an (x,y) index (dx', dy') into the threshold array to retrieve the threshold value to render the pixel at coordinated (dx, dy) utilizing the following equations:

dx'=(dx-n*offset) mod (w)

dy'=(dy-n*h)

where h is the height of the threshold array, w is the width of the threshold array and mod is a modular function.

Term	Documents
(4 AND 1).PGPB,USPT,EPAB,JPAB,DWPI,TDBD.	6
(L4 AND L1).PGPB,USPT,EPAB,JPAB,DWPI,TDBD.	6

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